wherein the transmission is initiated by the row selector circuit and the column selector circuit, which defines the intersection.

13. (new) A storage system suitable for storing a plurality of objects each associated with an identification device, said system comprising:

an assembly having a plurality of locations each of which are adapted to receive an identification device;

a two terminal electronic memory device associated with each identification device, each electronic memory device including a serially transmittable individualized code;

addressing logic; and

a logic circuit for receiving serial transmissions from an addressed identification device;

wherein the transmission is initiated by the addressing logic.

14. (new) A storage system suitable for storing a plurality of objects each associated with an identification device, said system comprising:

an assembly comprising a plurality of locations each of which are adapted to receive an identification device;

an electronic memory device, associated with each identification device, comprising a data connection, a ground return connection and a serially transmittable individualized code;

logic circuits for signaling the data connection of a selected electronic memory device; and

a logic circuit for receiving the serial transmission of the individualized code from an addressed electronic memory device.

15. (new) A storage system suitable for storing a plurality of objects each associated with an identification device, said system including an assembly having a plurality of locations each adapted to receive an identification device, said system comprising:

a two terminal electronic memory device, associated with an identification device, that includes a serially transmittable individualized code;

addressing logic to initiate transmissions of the individualized code from a selected memory device; and

a processor to receive the serially transmitted individualized code and associate an identification device with a location.

16. (new) A storage system suitable for storing a plurality of objects each associated with an identification device, said system comprising:

a plurality of mechanically coupled locations, each adapted to receive an identification device;

an electronic memory device, associated with each identification device, comprising a data connection and a ground return connection and a serially transmittable individualized code;

addressing logic;

a processor;

wherein the addressing logic signals a memory device via its data and ground return connections to transmit its individualized code and wherein the processor associates the individualized code with a location.

17. (new) A storage system suitable for storing a plurality of objects each associated with an identification device, a plurality of mechanically coupled locations adapted to receive an identification device, said system comprising:

an electronic memory device, associated with each identification device, comprising a data connection, a ground return connection and a serially transmittable individualized code;

addressing logic;

processing logic;

wherein the addressing logic signals a memory device via its data and ground return connections to transmit its individualized code, and wherein the processing logic associates the individualized code with a location.

18. (new) A storage system suitable for storing a plurality of objects each associated with an identification device, said system including an assembly having a plurality of locations each adapted to receive an identification device, said system comprising:

a two terminal electronic device associated with an identification device for transmitting an individualized code;

addressing logic to initiate transmissions from the electronic device; and

a processor to receive a transmitted individualized code and associate the identification device with a location.

19. (new) The system as claimed in claim 12, wherein the individualized code comprises a plurality of bits.

20. (new) The system as claimed in claim 13, wherein the individualized code comprises a plurality of bits.

21. (new) The system as claimed in claim 14, wherein the individualized code comprises a plurality of bits.

22. (new) The system as claimed in claim 15, wherein the individualized code comprises a plurality of bits.

23. (new) The system as claimed in claim 16, wherein the individualized code comprises a plurality of bits.

24. (new) The system as claimed in claim 17, wherein the individualized code comprises a plurality of bits.